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(54) **Communications system for communications between an electronic control apparatus and a test apparatus**

Kommunikationssystem zur Kommunikation zwischen elektronischem Kontrollapparat und Testapparat

Système de communication pour la communication entre un appareil de contrôle et un appareil de test

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Description

The present invention relates to a testing system for testing electronic control apparatus by sending and receiving data between test apparatus and said electronic control apparatus using serial asynchronous communications. The invention is applicable to a system connected to enable data sending and receiving between electronic control apparatus comprising a serial asynchronous communications function and test apparatus for checking the operation of said electronic control apparatus where the communications mode of the test apparatus differs from that of the electronic control apparatus.

One application for the invention is to enable data communications between a test apparatus and an automotive electronic control apparatus used for anitlock brake control, engine control, or other automotive applications.

US-A-4 879 831 describes a communications system for sending and receiving data between electronic apparatus having a serial communications function and further apparatus. The electronic apparatus initiates communication by transmitting a test signal prior to data transmission. The further apparatus responds to the test signal by transmitting a response signal to indicate whether it is capable of full duplex or half duplex communication. The electronic apparatus then responds to the response signal to select full duplex or half duplex communication accordingly.

One type of common electronic control apparatus today is the electronic control unit used in automobiles to control the antilock brake control system.

In such an application, the electronic control apparatus calculates the vehicle speed, acceleration/deceleration of each wheel, and other parameters based on the input signals output from wheel speed sensors and other devices. When wheel skidding is detected from the minimum detected wheel speed and from the relationship between vehicle speed and wheel speed, the electronic control apparatus outputs control signals to the solenoids and motors used to drive the reflux pump and other components to alleviate skidding. These electronic control apparatuses also typically store a troubleshooting code that identifies trouble spots when a problem develops in the wheel speed sensors or other components.

These electronic control systems are typically self-regulating with a test apparatus provided to check whether the control signals are output to the motor and solenoids, and to read the troubleshooting codes to confirm the identified problem area. In such systems, the electronic control apparatus and test apparatus are linked via a communications bus, and data is sent and received between the components using serial communications protocols.

Two serial communications formats are commonly used: full duplex in which two signal buses are used discretely for sending and receiving, and half duplex in which one signal bus is used for both sending and receiving. As a result, if the electronic control apparatus and the test apparatus do not use the same communications format, it is not possible for data to be sent between the two devices.

This is a particular problem in mobile electronic control apparatuses because the communications formats of the electronic control apparatus are often different in different models and vehicle makes. This makes it necessary to have test apparatuses compatible with the different communications formats of the electronic control units, resulting in increased cost and inconvenience.

Therefore, an object of the present invention is to resolve this incompatibility in communications formats between electronic control and test apparatuses by enabling data sending and receiving between an electronic control apparatus and test apparatuses with a communications format different from that of the connected electronic control apparatus.

According to the present invention, there is provided a testing system for testing electronic control apparatus by sending and receiving data between test apparatus and said electronic control apparatus using serial asynchronous communications, said test apparatus comprising: an identification terminal for outputting an identification signal indicative of either full duplex communications mode or half duplex communications mode; and said electronic control apparatus comprising: a communications circuit for receiving said identification signal and for setting either said full duplex communications mode or said half duplex communications mode depending on said identification signal, wherein said test apparatus is operable to initiate said serial asynchronous communications by outputting said identification signal.

In one embodiment, said test apparatus comprises: an identification signal generator means for generating only an identification signal indicative of full duplex communications mode; and a microcomputer having a terminal means for sending and receiving data according to a full duplex communications mode.

In another embodiment, said test apparatus comprises: an identification signal generator means for generating only an identification signal indicative of a half duplex communications mode; and a microcomputer having a terminal means for sending and receiving data according to half duplex communications mode.

The present invention will become more fully understood from the detailed description given below and the accompanying diagrams wherein:

Fig. 1 is a block diagram of an electronic control apparatus connected to a full duplex test apparatus according to the present invention,

Fig. 2 is a block diagram of an electronic control apparatus connected to a half duplex test apparatus according to the present invention, and

Fig. 3 is a flow chart of the communications control sequence of the invention.

The present invention is described below based on the preferred embodiment shown in the figures.

As shown in Figs. 1 and 2, either a full duplex test apparatus 2 or a half duplex test apparatus 3 can be connected to the electronic control apparatus 1, and data is serially transmitted between the electronic control apparatus 1 and the connected test apparatus 2 or 3.

The electronic control apparatus 1 of this embodiment is an electronic control apparatus used in a motor vehicle, and comprises a microprocessor 5 with an asynchronous serial communications function. The microprocessor 5 further comprises a memory M1 for storing a troubleshooting code identifying the trouble spot when a problem develops in any of the components of the antilock brake control system, including the motor and solenoids (not shown in the figures). The microprocessor 5 processes the signals input from the wheel speed sensors and other components based on an antilock control algorithm, and outputs control signals to the motor, solenoids, and other system components accordingly.

The microprocessor 5 in the electronic control apparatus 1 further comprises both full duplex sender 6 and receiver 7, and half duplex sender 8 and receiver 9. The full and half duplex senders 6 and 8 are connected to the serial transmission terminal Tx of the microprocessor 5 through respective first and second gates 11 and 12.

The microprocessor 5 port terminal Port voltage is input to both the first and second gates 11 and 12. When the Port voltage is HIGH, the first gate 11 opens, enabling the signal to flow from the full duplex sender 6 to the serial transmission terminal Tx. When the port terminal Port is connected to the ground, i.e., when the port terminal Port voltage is LOW, the second gate 12 opens, enabling the signal to flow from the half duplex sender 8 to the serial transmission terminal Tx.

The full and half duplex receiver 7 and 9 are similarly connected to the serial receiving terminal Rx of the microprocessor 5 through respective third and fourth gates 13 and 14.

The microprocessor 5 port terminal Port voltage is also input to both the third and fourth gates 13 and 14. When the Port voltage is HIGH, the third gate 13 opens, enabling the signal to flow to the full duplex receiver 7 from the serial receiving terminal Rx. When the port terminal Port voltage is LOW, the fourth gate 14 opens, enabling the signal to flow to the half duplex receiver 9 from the serial receiving terminal Rx.

The electronic control apparatus 1 microprocessor 5 is programmed as shown in Fig. 3 to select the appropriate communications control program according to the voltage signal input to the port terminal Port.

Referring to Fig. 3, the input voltage to the port terminal Port is read at step #1, and the HIGH/LOW state of this voltage is evaluated at step #2. If the port terminal Port voltage is HIGH (+Vcc), the microprocessor 5 selects the full duplex communications control program (step #3), but if the Port voltage is LOW (ground), the microprocessor 5 selects the half duplex communications control program (step #4). After the communications control program is thus adaptively selected, the microprocessor 5 proceeds to the normal data sending/receiving sequence between the test apparatuses 2, 3 (step #5).

Note that while the serial transmission terminal Tx, serial receiving terminal Rx, and port terminal Port are provided in the microprocessor 5 of the electronic control apparatus 1, these terminals are connected by a communications circuit of fifth, sixth, and seventh gates 15, 16, 17 to the first and second external communications terminals A1, B1 and detection terminal C1 used to connect the electronic control apparatus 1 to the test apparatus 2 or 3.

The serial transmission terminal Tx is connected through the fifth gate 15 to the first external communications terminal A1, thus controlling the signal flow from the serial transmission terminal Tx to the first external communications terminal A1.

The serial receiving terminal Rx is similarly connected through the sixth gate 16 to the second external communications terminal B1, thus controlling the signal flow from the second external communications terminal B1 to the serial receiving terminal Rx.

The port terminal Port is connected directly to the detection terminal C1.

A bypass line 18 with the seventh gate 17 connects the bus between the first external communications terminal A1 and fifth gate 15 to the bus between the second external communications terminal B1 and the sixth gate 16. The detection terminal C1 voltage is input to the seventh gate 17, which opens when the input voltage is LOW to permit the signal to flow from the first external communications terminal A1 to the serial receiving terminal Rx.

The full duplex test apparatus 2 shown in Fig. 1 comprises a microprocessor 19 for processing the troubleshooting code read from the electronic control apparatus 1, and outputs operational check signals to the electronic control apparatus 1.

The microprocessor 19 further comprises a serial receiving terminal Rx' and a serial transmission terminal Tx', and these terminals are respectively connected to the first and second communications terminals A2, B2 used to connect the full duplex test apparatus 2 to the electronic control apparatus 1.

A gate 21 is provided between the serial receiving terminal Rx' and the first external communications terminal A2 to pass signals one way only into the serial receiving terminal Rx'. Another gate 22 is similarly connected between the serial transmission terminal Tx' and the second external communications terminal B2 to pass signals one way only from the serial transmission

terminal Tx' to the second external communications terminal B2.

This full duplex test apparatus 2 further comprises an identification terminal C2 for connection with the detection terminal C1 of the electronic control apparatus 1. The identification terminal C2 is connected to a voltage supply 23 in the test apparatus 2, and continuously outputs a HIGH voltage signal.

The half duplex test apparatus 3 shown in Fig. 2 similarly comprises a microprocessor 25 with a serial receiving terminal Rx" and a serial transmission terminal Tx".

The half duplex test apparatus 3 also comprises an external communications terminal A3 and an identification terminal C3 for connection with the first external communications terminal A1 and detection terminal C1, respectively, of the electronic control apparatus 1.

The external communications terminal A3 is connected to both the serial receiving Rx" and serial transmission Tx" terminals through gates 26 and 27, respectively. These gates 26 and 27 respectively regulate the signal flow either from the external communications terminal A3 into the serial receiving terminal Rx", or from the serial transmission terminal Tx" to the external communications terminal A3 only.

The identification terminal C3 is connected to the ground 28, and the voltage signal from the identification terminal C3 is always LOW.

The operating features of this embodiment of the invention are described below.

The first case to consider is the connection of the electronic control apparatus 1 to a full duplex test apparatus 2 as shown in Fig. 1. In this case, the first external communications terminal A1, second external communications terminal B1, and detection terminal C1 of the electronic control apparatus 1 are connected to the first external communications terminal A2, second external communications terminal B2, and identification terminal C2 of the full duplex test apparatus 2, respectively.

Because the identification terminal C2 always outputs a HIGH voltage signal as described above, a positive voltage is input to the first through fourth gates 11, 12, 13, 14, and the seventh gate 17 of the electronic control apparatus 1.

This HIGH voltage causes the first and third gates 11, 13 to open and pass the signal, and the second, fourth, and seventh gates 12, 14, 17 to close and impede the signal flow. As a result, signals can flow from the full duplex sender 6 through the serial transmission terminal Tx to the first external communications terminal A1, and from the second external communications terminal B1 through the serial receiving terminal Rx to the full duplex receiver 7 when the electronic control apparatus 1 is connected to a full duplex test apparatus 2.

As a result, when a full duplex test apparatus 2 is connected to the electronic control apparatus 1, the communications circuit of the electronic control apparatus 1 is automatically set to the full duplex communications mode.

As previously described, however, it is also possible to connect the electronic control apparatus 1 to a half duplex test apparatus 3.

In this case, the external communications terminal A3 and identification terminal C3 of the half duplex test apparatus 3 connect with the first external communications terminal A1 and detection terminal C1, respectively, of the electronic control apparatus 1. Because the half duplex test apparatus 3 identification terminal C3 is connected to the ground 28, a LOW voltage is output to the first through fourth gates 11, 12, 13, 14, and the seventh gate 17 of the electronic control apparatus 1. This LOW voltage causes the first and third gates 11, 13 to close and impede the signal flow, and the second, fourth, and seventh gates 12, 14, 17 to open and pass the signal flow. The signal from the half duplex sender 8 therefore flows through the serial transmission terminal Tx to the first external communications terminal A1, and signals input from the first external communications terminal A1 flow through the seventh gate 17 and serial receiving terminal Rx into the half duplex receiver 9.

When the port terminal Port detects a LOW voltage signal at the identification terminal C3 of the connected half duplex test apparatus 3, the microprocessor 5 sets the communications control program to the half duplex mode to enable data sending and receiving between the electronic control apparatus 1 and the half duplex test apparatus 3 in the same way communications is controlled with the full duplex test apparatus 2 connection described above.

As a result, when a half duplex test apparatus 3 is connected to the electronic control apparatus 1, the communications circuit of the electronic control apparatus 1 is automatically set to the half duplex communications mode.

It is to be noted that the present invention shall not be limited to the embodiment described above, and variations are possible as will be obvious to those skilled in the art. For example, the electronic control apparatus of the present embodiment is described as a mobile electronic control apparatus for antilock brake system control, but it can also be used for engine control and is not necessarily limited to automotive applications. In addition, the gates in the internal microprocessor of the electronic control apparatus are directly controlled by the signal from the identification terminal of the test apparatus, but the gates may alternatively be controlled in software by the communications control program, for example.

In addition, a HIGH voltage signal at the identification terminal is used to identify a full duplex test apparatus, and a ground voltage signal at the identification terminal is used to identify a half duplex test apparatus, but the voltage signals of the test apparatus identification terminal can in practice be any signals enabling positive recognition of the full or half duplex communications mode.

As will be known from the above description, the system enabling communications between an electronic control apparatus and test apparatus according to the invention comprises in the test apparatus an identification terminal outputting different signals according to the full or half duplex communications mode used by the test apparatus, and sets the communications circuit of the electronic control apparatus to enable communications with the test apparatus by determining the communications mode of the test apparatus from the signal output from the identification terminal. The electronic control apparatus is therefore able to send and receive data with both full and half duplex test apparatuses. It is thus possible by means of the present invention to connect plural test apparatuses using different communications modes to a single electronic control apparatus, thereby enabling universal use of the test apparatus and reducing costs.

Specifically, the test apparatus comprises a communications terminal for connecting with the electronic control apparatus, and an identification terminal for outputting a voltage signal identifying whether the communications mode of the test apparatus is full or half duplex. The electronic control apparatus comprises both full and half duplex sending and receiving means, and a detection terminal for connection with the identification terminal of the test apparatus. The sending and receiving means are connected by the communications circuit to the external communications terminal through gates, and the gates are opened or closed according to the voltage input to the detection terminal. The connection terminal of the test apparatus is connected to the external communications terminal of the electronic control circuit, and the identification terminal of the test apparatus is connected to the detection terminal of the electronic control circuit. Based on the voltage signal input from the identification terminal to the detection terminal, either the gate between the external communications terminal and the full duplex sending/receiving means is opened, or the gate between the external communications terminal and the half duplex sending/receiving means is opened.

Because the communications system for communications between an electronic control apparatus and test apparatus is thus arranged, the electronic control apparatus can determine whether the communications mode of the test apparatus is full or half duplex based on the signal output by the identification terminal of the test apparatus, and the communications circuit is set accordingly to either full or half duplex.

More specifically, a gate means is provided in the communications circuit connecting the external communications terminal to the full duplex sending/receiving means and the half duplex sending/receiving means, and the voltage from the identification terminal is input to the gate means to connect the sending/receiving means matching the communications format of the test apparatus to the external communications terminal.

Using the present system, it is also not necessary to change the communications circuit or other components of the electronic control apparatus when the communications mode of the test apparatus is changed.

In addition, the present system offers the advantage of achieving the effect described above by means of a simple construction, requiring only an identification terminal outputting a voltage signal corresponding to the communications mode of the test apparatus, and gates that are opened and closed based on this voltage signal in the communications circuit of the electronic control apparatus.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the scope of the invention which is defined by the appended claims, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

Claims

1. A testing system for testing electronic control apparatus (1) by sending and receiving data between test apparatus (2) and said electronic control apparatus (1) using serial asynchronous communications, said test apparatus (2) comprising:

   an identification terminal (C2) for outputting an identification signal indicative of either full duplex communications mode or half duplex communications mode; and
   said electronic control apparatus (1) comprising:
   a communications circuit (11, 12, 13, 14, 17) for receiving said identification signal and for setting either said full duplex communications mode or said half duplex communications mode depending on said identification signal, wherein
   said test apparatus (2) is operable to initiate said serial asynchronous communications by outputting said identification signal.

2. A testing system according to claim 1 wherein

   said test apparatus (2) comprises:
   an identification signal generator means (23) generating an identification signal indicative of full duplex communications mode; and
   a microcomputer (19) having a terminal means (A_2, B_2) for sending and receiving data according to a full duplex communications mode.

3. A testing system according to claim 1 wherein

   said test apparatus (2) comprises:

an identification signal generator means (28) generating an identification signal indicative of a half duplex communications mode; and
a microcomputer (25) having a terminal means (A_3) for sending and receiving data according to half duplex communications mode.

Patentansprüche

1. Ein Testsystem zum Testen einer elektronischen Steuervorrichtung (1) durch Senden und Empfangen von Daten zwischen Testvorrichtung (2) und der elektronischen Steuervorrichtung (1), unter Verwendung serieller asynchroner Kommunikation, wobei die Testvorrichtung (2) umfaßt:

   einen Identifikationsanschluß (C2) zum Ausgeben eines Identifikationssignals, das entweder auf einen Vollduplex-Kommunikationsmodus oder einen Halbduplex-Kommunikationsmodus hindeutet; und die elektronische Steuervorrichtung (1) umfaßt:

   eine Kommunikationsschaltung (11, 12, 13, 14, 17) zum Empfangen des Identifikationssignals, und zum Einstellen entweder des Vollduplex-Kommunikationsmodus oder des Halbduplex-Kommunikationsmodus, abhängend von dem Identifikationssignal, wobei

   die Testvorrichtung (2) zum Initiieren der seriellen asynchronen Kommunikation durch Ausgeben des Identifikationssignals betreibbar ist.

2. Ein Testsystem nach Anspruch 1,
   dadurch gekennzeichnet, daß

   die Testvorrichtung (2) umfaßt:

   eine Identifikationssignal-Erzeugungseinrichtung (23), die ein Identifikationssignal erzeugt, das auf Vollduplex-Kommunikationsmodus hindeutet; und

   einen Mikrocomputer (19) mit einer Anschlußeinrichtung (A_2, B_2) zum Senden und Empfangen von Daten entsprechend einem Vollduplex-Kommunikationsmodus.

3. Ein Testsystem nach Anspruch 1,
   dadurch gekennzeichnet, daß

   die Testvorrichtung (2) umfaßt:

   eine Identifikationssignal-Erzeugungseinrichtung (28), die ein Identifikationssignal erzeugt, das auf einen Halbduplex-Kommunikationsmodus hindeutet; und

   einen Mikrocomputer (25) mit einer Anschlußeinrichtung (A_3) zum Senden und Empfangen von Daten entsprechend einem Halbduplex-Kommunikationsmodus.

Revendications

1. Système de test pour tester un appareil de commande électronique (1) en envoyant et en recevant des données entre un appareil de test (2) et ledit appareil de commande électronique (1) en utilisant une communication asynchrone série, ledit appareil de test (2) comprenant :

   une borne d'identification (C2) pour émettre en sortie un signal d'identification indicatif de soit un mode communication duplex complet, soit un mode communication semi-duplex ; et
   ledit appareil de commande électronique (1) comprenant :
   un circuit de communication (11, 12, 13, 14, 17) pour recevoir ledit signal d'identification et pour établir soit ledit mode communication duplex complet, soit ledit mode communication semi-duplex en fonction dudit signal d'identification, dans lequel :
   ledit appareil de test (2) peut fonctionner pour initier ladite communication asynchrone série en émettant en sortie ledit signal d'identification.

2. Système de test selon la revendication 1, dans lequel :

   ledit appareil de test (2) comprend :
   un moyen de générateur de signal d'identification (23) qui génère un signal d'identification indicatif d'un mode communication duplex complet ; et
   un micro-ordinateur (19) comportant un moyen de borne (A_2, B_2) pour envoyer et recevoir des données conformément à un mode communication duplex complet.

3. Système de test selon la revendication 1, dans lequel ledit appareil de test (2) comprend :

   un moyen de générateur de signal d'identification (28) qui génère un signal d'identification indicatif d'un mode communication semi-duplex ; et
   un micro-ordinateur (25) comportant un moyen de borne (A_3) pour envoyer et recevoir des données conformément à un mode communication semi-duplex.

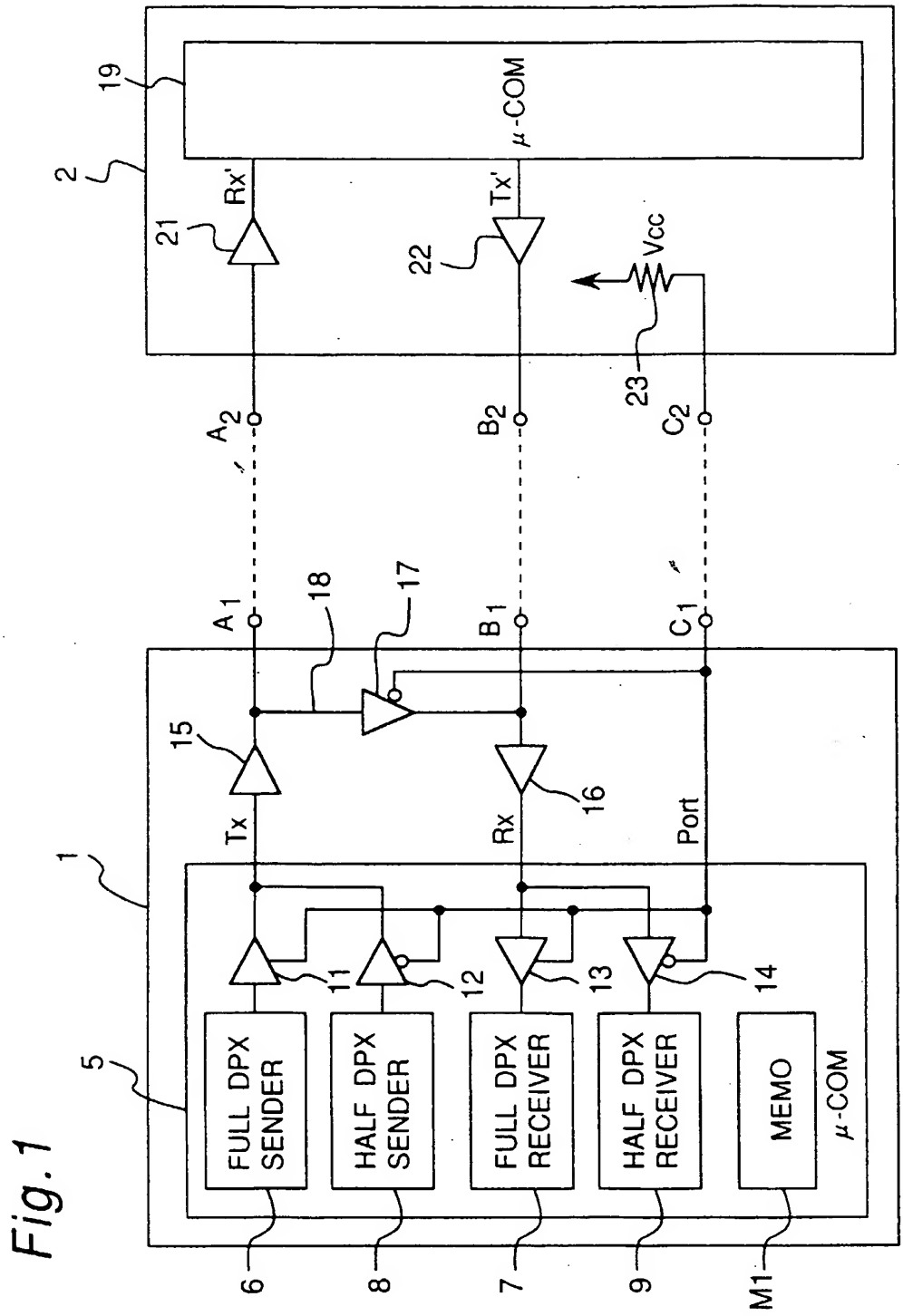
19
2
μ-COM
21
Rx'
22
Tx'
Vcc
23
A2
B2
C2
A1
18
17
B1
C1
15
16
Tx
Rx
Port
1
11
12
13
14
5
FULL DPX SENDER
HALF DPX SENDER
FULL DPX RECEIVER
HALF DPX RECEIVER
MEMO
μ-COM
6
8
7
9
M1

Fig. 1

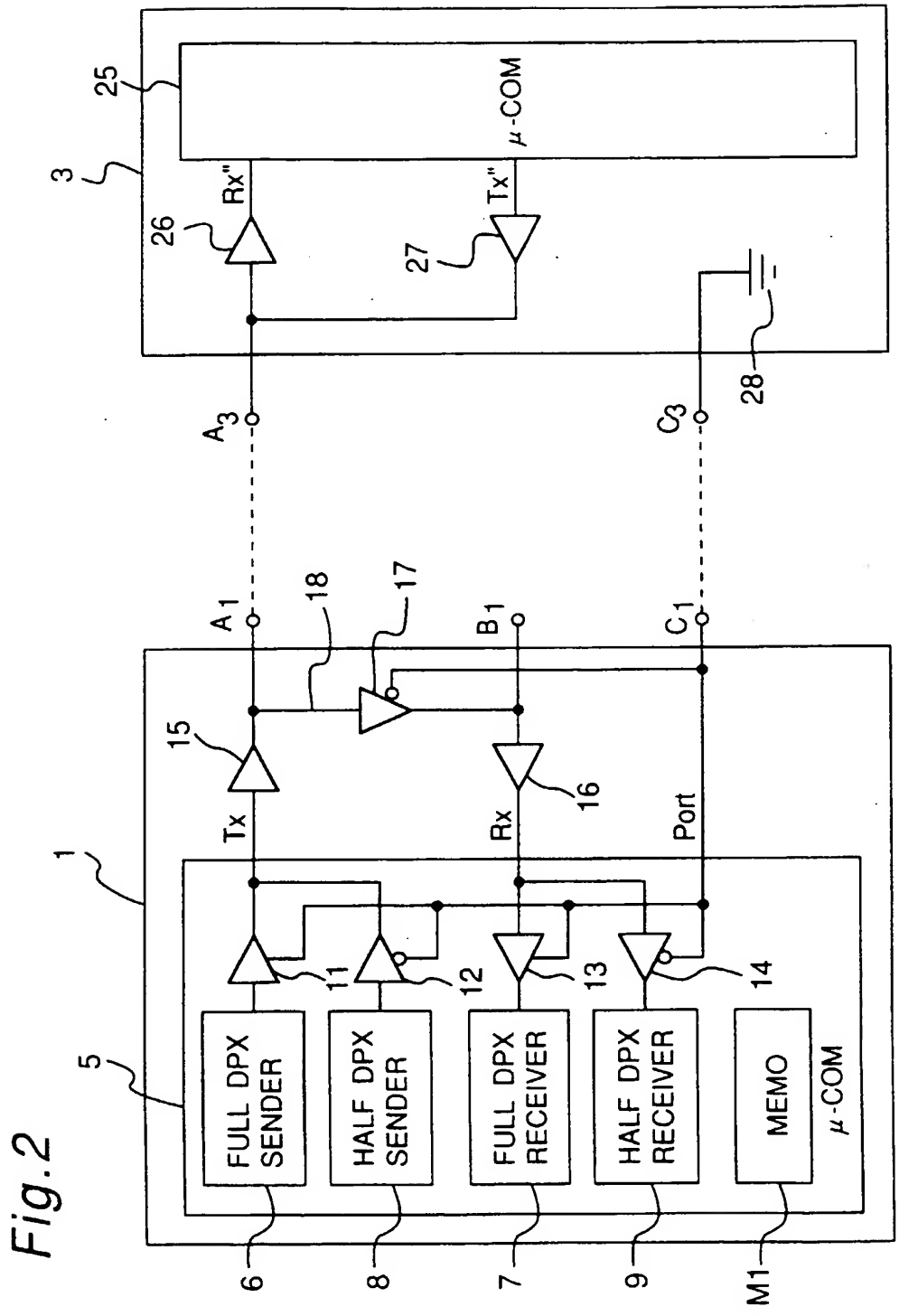
25
μ-COM
3
Rx"
Tx"
26
27
28
A3
C3
A1
18
17
B1
C1
15
16
Tx
Rx
Port
1
11
12
13
14
5
FULL DPX SENDER
HALF DPX SENDER
FULL DPX RECEIVER
HALF DPX RECEIVER
MEMO
μ-COM
6
8
7
9
M1

Fig.2

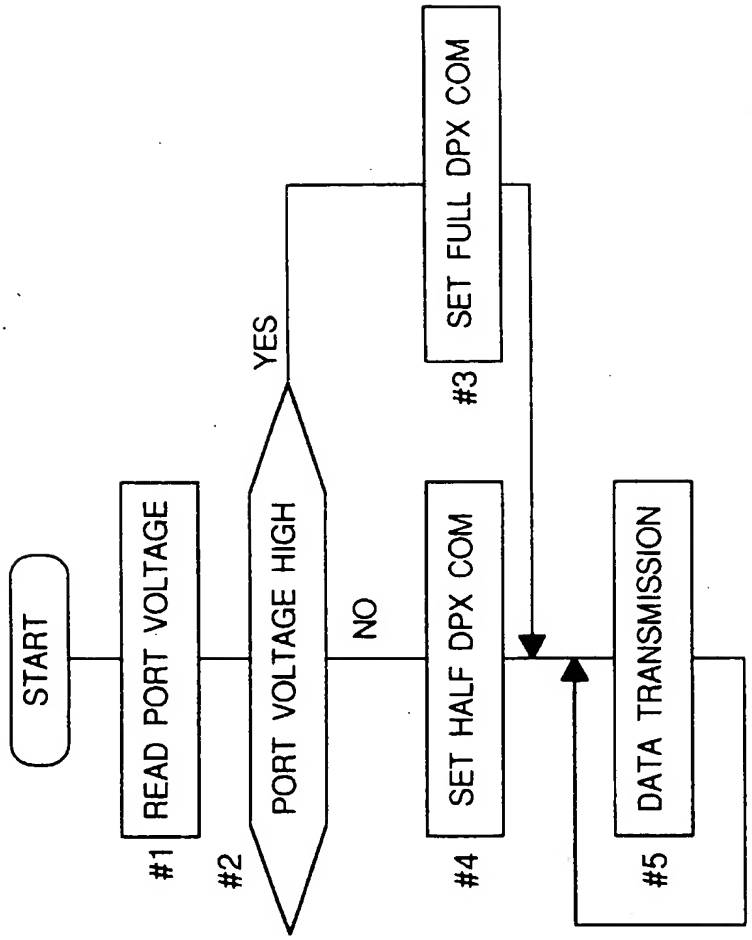
START
READ PORT VOLTAGE
#1
PORT VOLTAGE HIGH
#2
YES
NO
SET FULL DPX COM
#3
SET HALF DPX COM
#4
DATA TRANSMISSION
#5

Fig.3